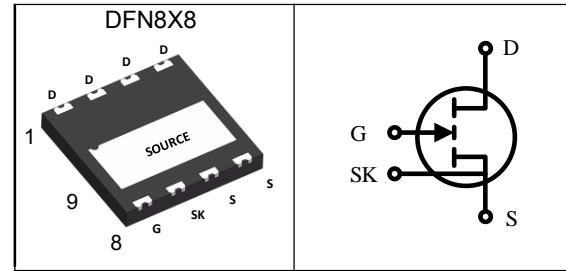


**650V GaN Enhancement-mode Power Transistor**
**Features**

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- RoHS, Pb-free-compliant

**Pin Description**

**Applications**

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion

$V_{DSS}$	650	V
$R_{DS(ON)-Typ}$	165	m $\Omega$
$I_D$	10	A

**Absolute Maximum Ratings** ( $T_C=25^\circ\text{C}$ , Unless Otherwise Noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-Source Voltage	650	V
$V_{GSS}$	Gate source voltage, continuous	-1.4 to +7	V
$V_{GSS,pulse}$	Gate source voltage, pulsed	$\pm 20$	V
$T_J$	Maximum Junction Temperature	-55 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$I_{D,pulse}$	Pulse Drain Current Tested	18	A
$I_D$	Continuous Drain Current	10	A
$P_D$	Maximum Power Dissipation	75	W

**Thermal Characteristics**

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	58.5	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance-Junction to Case	1.65	$^\circ\text{C}/\text{W}$



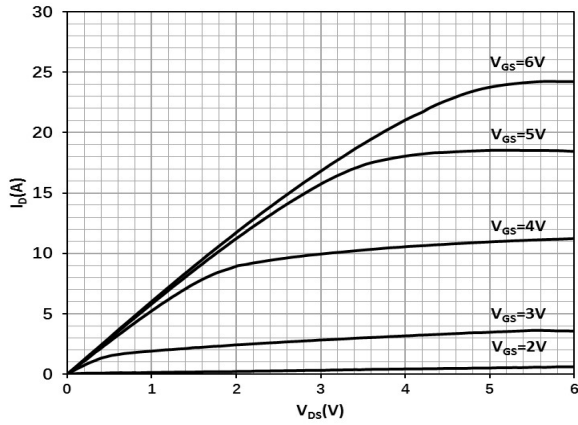
**650V GaN Enhancement-mode Power Transistor**

**Electrical Characteristics** ( $T_J=25^{\circ}\text{C}$ , Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Static Electrical Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	---	---	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=650V, V_{GS}=0V$	---	0.4	20	$\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=11mA$	1.2	1.7	2.5	V
$I_{GSS}$	Gate Leakage Current	$V_{GS}=6V, V_{DS}=0V$	---	50	---	$\mu A$
$R_{DS(ON)}$	Drain-Source On-state Resistance	$V_{GS}=6V, I_D=3A$	---	165	240	$m\Omega$
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=400V, V_{GS}=0V, \text{Freq.}=1MHz$	---	79	---	pF
$C_{oss}$	Output Capacitance		---	25	---	
$C_{riss}$	Reverse Transfer Capacitance		---	0.2	---	
$C_{o(er)}$	Effective output capacitance, energy related	$V_{DS}=0 \text{ to } 400V, V_{GS}=0V$	---	36	---	pF
$C_{o(tr)}$	Effective output capacitance, time related		---	52	---	
$Q_{OSS}$	Output charge	$V_{DS}=0 \text{ to } 400V, V_{GS}=0V$	---	21	---	nC
$T_{d(on)}$	Turn-on Delay Time	$V_{DS}=400V, V_{GS}=6V, I_D=6A, R_{on}=10\Omega, R_{off}=2\Omega$	---	2	---	nS
$T_r$	Turn-on Rise Time		---	5	---	
$T_{d(off)}$	Turn-off Delay Time		---	4	---	
$T_f$	Turn-off Fall Time		---	6	---	
$Q_g$	Total Gate Charge	$V_{DS}=400V, V_{GS}=6V, I_D=3A$	---	2	---	nC
$Q_{gs}$	Gate-Source Charge		---	0.2	---	
$Q_{gd}$	Gate-Drain Charge		---	0.7	---	
<b>Source-Drain Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_S=3A, V_{GS}=0V$	---	2.6	---	V
$I_{S, pulse}$	Pulsed current, reverse	$V_{GS}=6V; t_{PULSE}=300\mu s$	---	---	18	A
$t_{rr}$	Reverse Recovery Time	$I_S=3A, V_{DS}=400V$	---	0	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	0	---	nC
$I_{rrm}$	Peak reverse recovery current		---	0	---	A

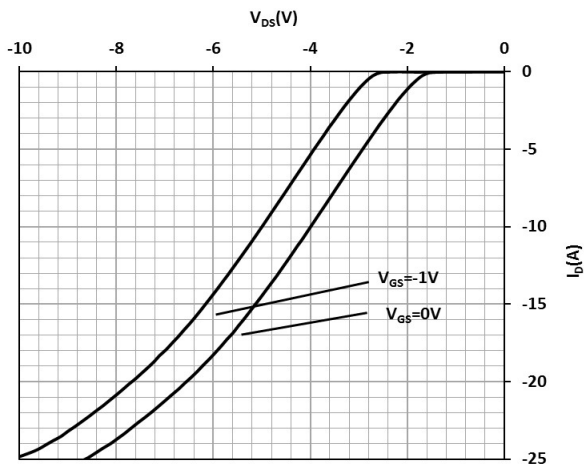
**650V GaN Enhancement-mode Power Transistor**
**Typical Characteristics**

Figure 1 Typ. output characteristics



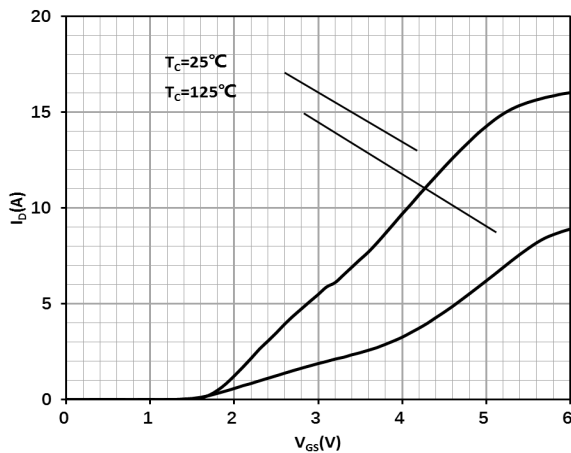
$$I_D = f(V_{DS}, V_{GS}); T_j = 25^\circ\text{C}$$

Figure 5 Typ. channel reverse characteristics



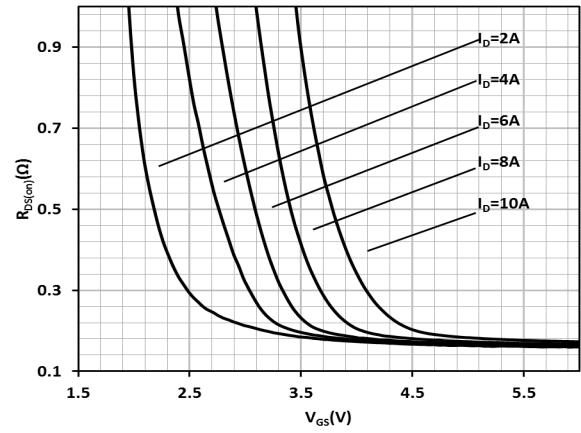
$$I_D = f(V_{DS}, V_{GS}); T_j = 25^\circ\text{C}$$

Figure 9 Typ. transfer characteristics



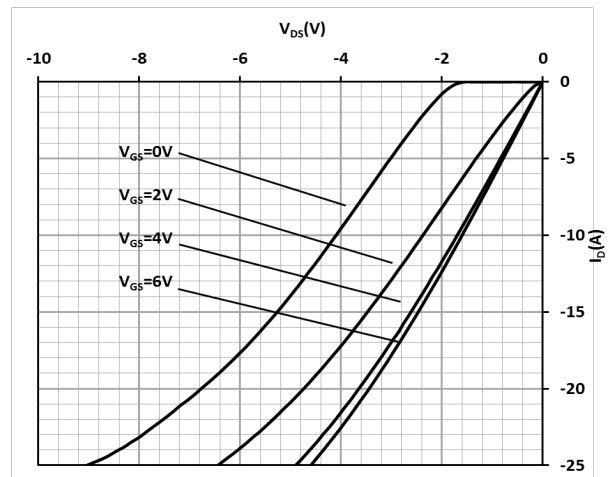
$$I_D = f(V_{GS}); V_{DS} = 3\text{V}$$

Figure 3 Typ. Drain-source on-state resistance



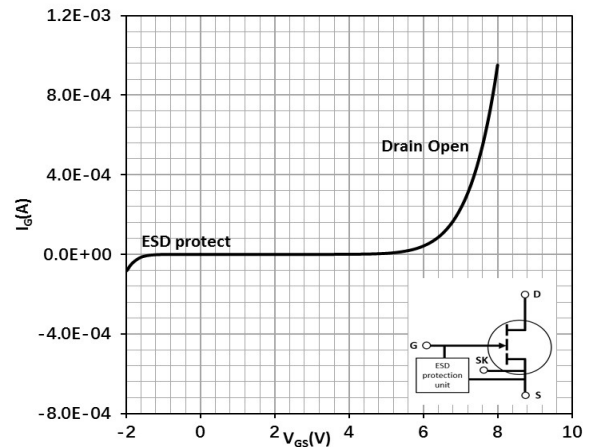
$$R_{DS(on)} = f(I_D, V_{GS}); T_j = 25^\circ\text{C}$$

Figure 7 Typ. channel reverse characteristics

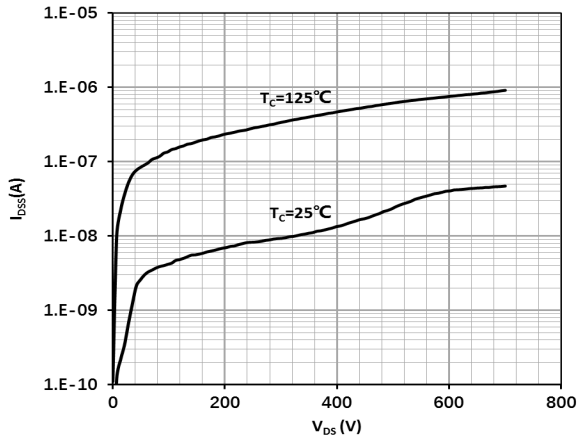


$$I_D = f(V_{DS}, V_{GS}); T_j = 25^\circ\text{C}$$

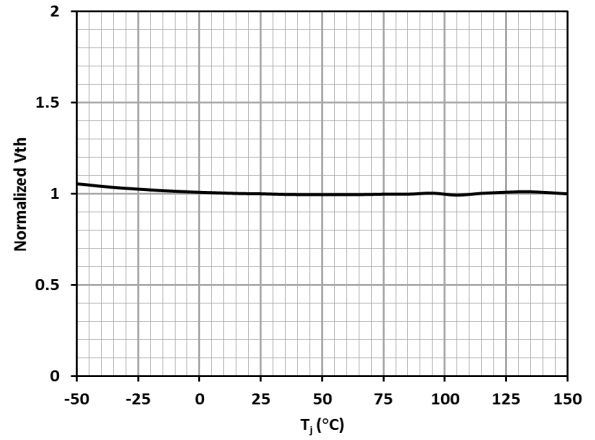
Figure 10 Typ. Gate-to-Source leakage



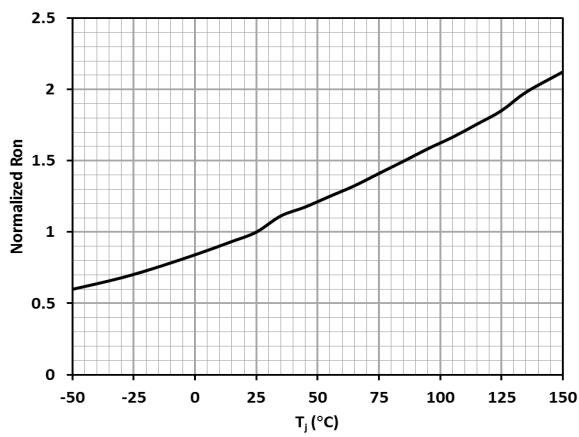
$$I_G = f(V_{GS}); I_G \text{ reverse turn on by ESD unit}$$

**650V GaN Enhancement-mode Power Transistor**
**Figure 11 Drain-source leakage characteristics**


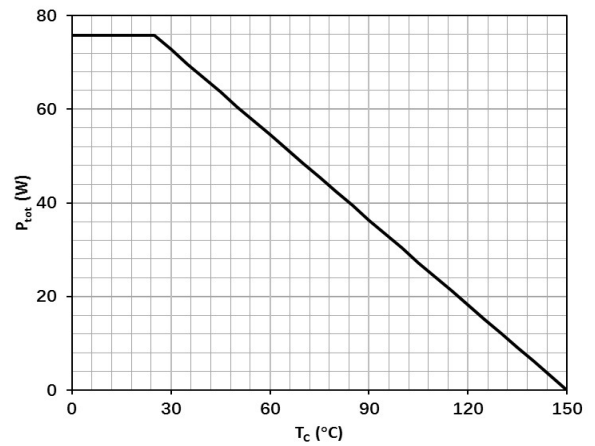
$$I_{DSS} = f(V_{DS}); V_{GS} = 0\text{ V}$$

**Figure 12 Gate threshold voltage**


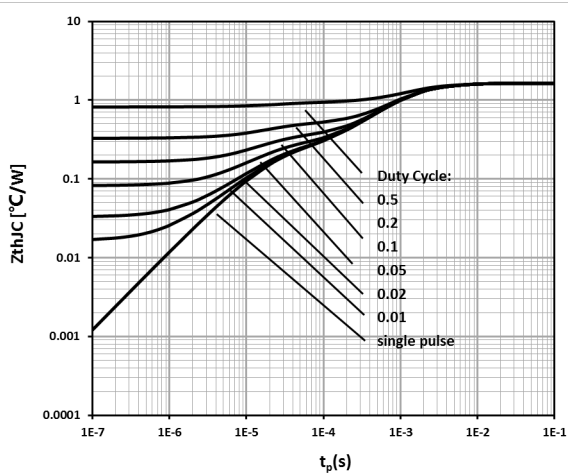
$$V_{TH} = f(T_j); V_{GS} = V_{DS}; I_D = 11\text{ mA}$$

**Figure 13 Drain-source on-state resistance**


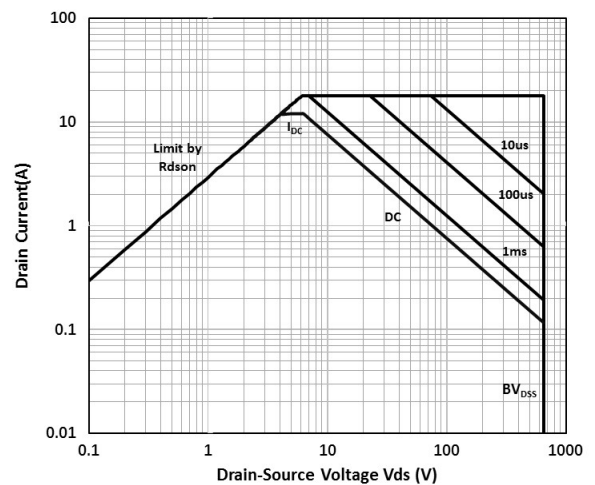
$$R_{DS(on)} = f(T_j); I_D = 3\text{ A}; V_{GS} = 6\text{ V}$$

**Figure 14 Power dissipation**


$$P_{tot} = f(T_c)$$

**Figure 15 Max.transient thermal impedance**


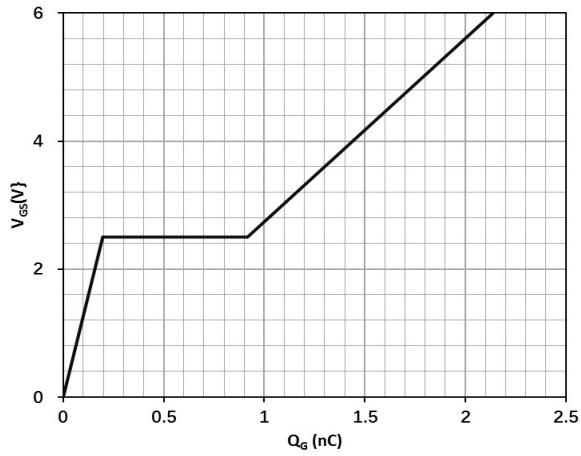
$$Z_{thJC} = f(t_p, D)$$

**Figure 16 Safe operating area**


$$I_D = f(V_{DS}); T_c = 25\text{ °C}$$

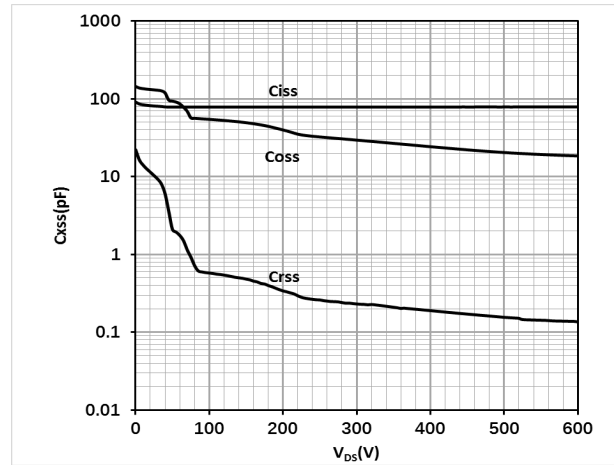
**650V GaN Enhancement-mode Power Transistor**

Figure 18 Typ. gate charge



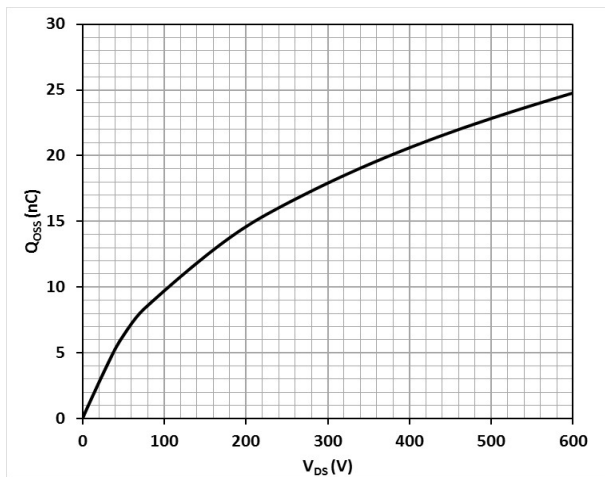
$$V_{GS} = f(Q_G); V_{DCLINK} = 400 \text{ V}; I_D = 3 \text{ A}$$

Figure 19 Typ. capacitances



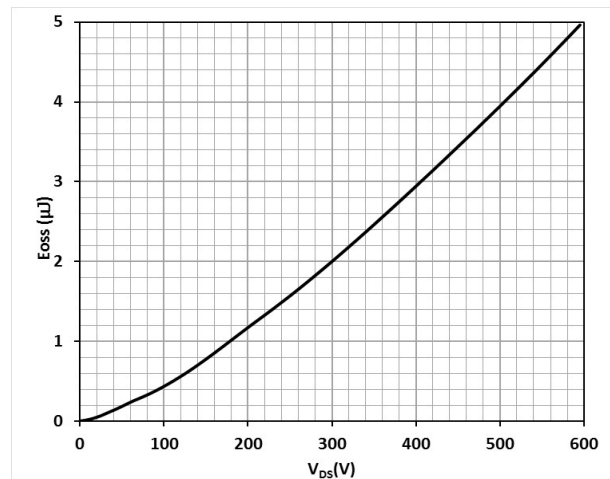
$$C_{XSS} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$$

Figure 20 Typ. output charge

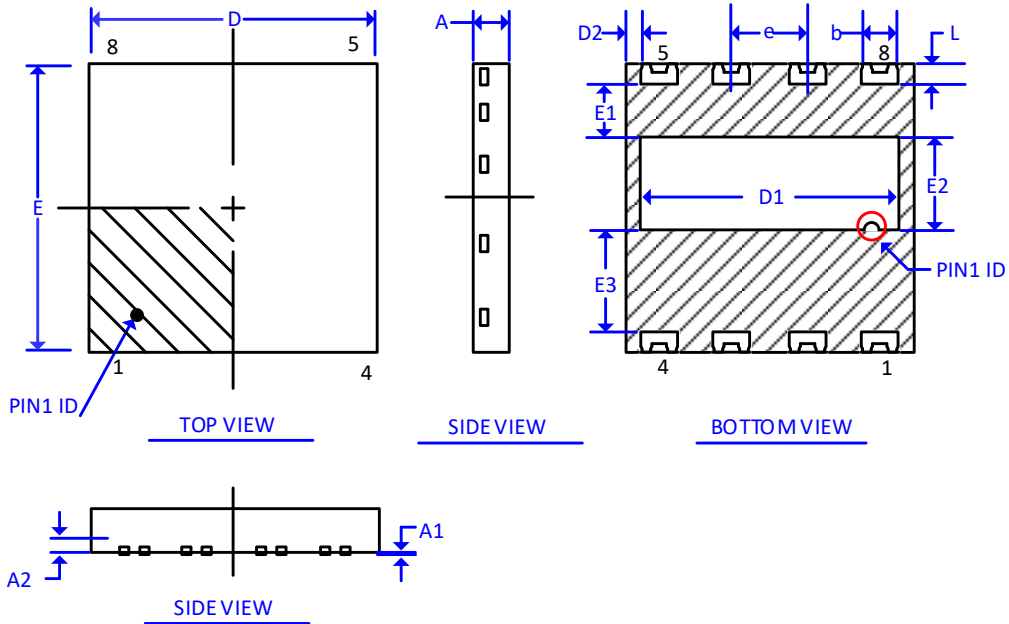


$$Q_{OSS} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$$

Figure 21 Typ. Coss stored Energy



$$E_{OSS} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$$

**650V GaN Enhancement-mode Power Transistor**
**DFN8X8 Package Outline Dimensions**


SYMBOL	DIMENSION			SYMBOL	DIMENSION		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.80	0.90	1.00	E	8.00 B.S.C		
A1	0.00	0.02	0.05	E1	0.90	1.00	1.10
A2	---	0.203 ref	---	E2	3.10	3.20	3.30
b	0.92	1.00	1.05	E3	2.70	2.80	2.90
D	8.00 B.S.C			e	2.00 B.S.C		
D1	6.84	6.94	7.04	L	0.40	0.50	0.60
D2	0.40	0.50	0.60				