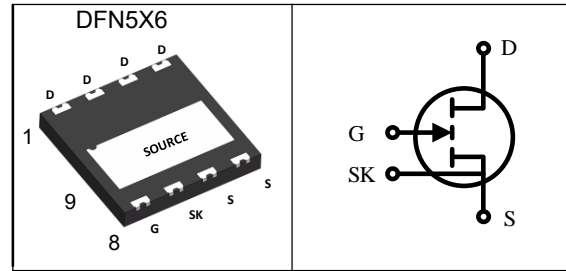


650V GaN Enhancement-mode Power Transistor
Features

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- RoHS, Pb-free-compliant

Pin Description

Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion

V_{DSS}	650	V
$R_{DS(ON)-Typ}$	106	m Ω
I_D	17	A

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	650	V
V_{GSS}	Gate source voltage, continuous	-1.4 to +7	V
$V_{GSS,pulse}$	Gate source voltage, pulsed	± 20	V
T_J	Maximum Junction Temperature	-55 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$I_{D,pulse}$	Pulse Drain Current Tested	32	A
I_D	Continuous Drain Current	17	A
P_D	Maximum Power Dissipation	113	W

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	60.3	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance-Junction to Case	1.1	$^\circ\text{C}/\text{W}$



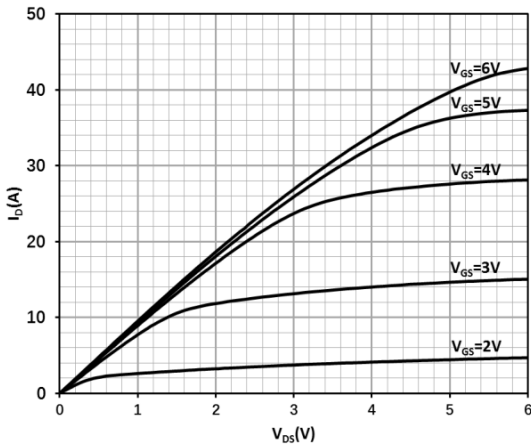
650V GaN Enhancement-mode Power Transistor

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=650V, V_{GS}=0V$	---	0.6	25	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=17.2mA$	1.2	1.7	2.5	V
I_{GSS}	Gate Leakage Current	$V_{GS}=6V, V_{DS}=0V$	---	70	---	μA
$R_{DS(ON)}$	Drain-Source On-state Resistance	$V_{GS}=6V, I_D=5A$	---	106	140	$m\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=400V,$ $V_{GS}=0V,$ Freq.=1MHz	---	125	---	pF
C_{oss}	Output Capacitance		---	41	---	
C_{rss}	Reverse Transfer Capacitance		---	0.4	---	
$C_{o(er)}$	Effective output capacitance, energy related	$V_{DS}=0$ to 400V, $V_{GS}=0V$	---	59	---	pF
$C_{o(tr)}$	Effective output capacitance, time related		---	82	---	
Q_{OSS}	Output charge	$V_{DS}=0$ to 400V, $V_{GS}=0V$	---	33	---	nC
$T_{d(on)}$	Turn-on Delay Time	$V_{DS}=400V, V_{GS}=6V,$ $I_D=10A, R_{on}=10\Omega, R_{off}=2\Omega$	---	3	---	nS
T_r	Turn-on Rise Time		---	5	---	
$T_{d(off)}$	Turn-off Delay Time		---	4	---	
T_f	Turn-off Fall Time		---	4	---	
Q_g	Total Gate Charge	$V_{DS}=400V, V_{GS}=6V, I_D=5A$	---	3.5	---	nC
Q_{gs}	Gate-Source Charge		---	0.3	---	
Q_{gd}	Gate-Drain Charge		---	1.2	---	
Source-Drain Characteristics						
V_{SD}	Diode Forward Voltage	$I_S=5A, V_{GS}=0V$	---	2.4	---	V
$I_{S, pulse}$	Pulsed current, reverse	$V_{GS} = 6V; t_{PULSE} = 300 \mu s$	---	---	32	A
t_{rr}	Reverse Recovery Time	$I_S=5A, V_{DS}=400V$	---	0	---	nS
Q_{rr}	Reverse Recovery Charge		---	0	---	nC
I_{rm}	Peak reverse recovery current		---	0	---	A

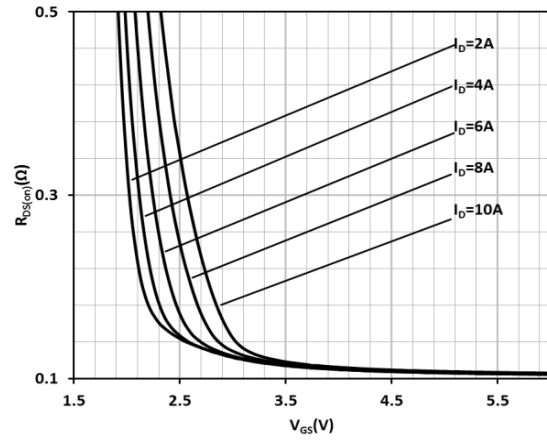
650V GaN Enhancement-mode Power Transistor
Typical Characteristics

Figure 1 Typ. output characteristics



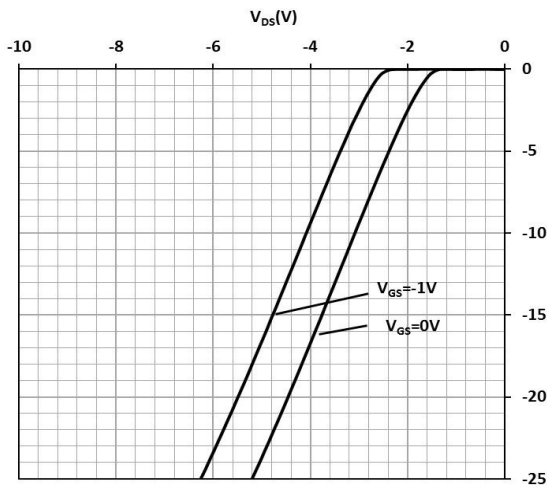
$$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^\circ\text{C}$$

Figure 2 Typ. Drain-source on-state resistance



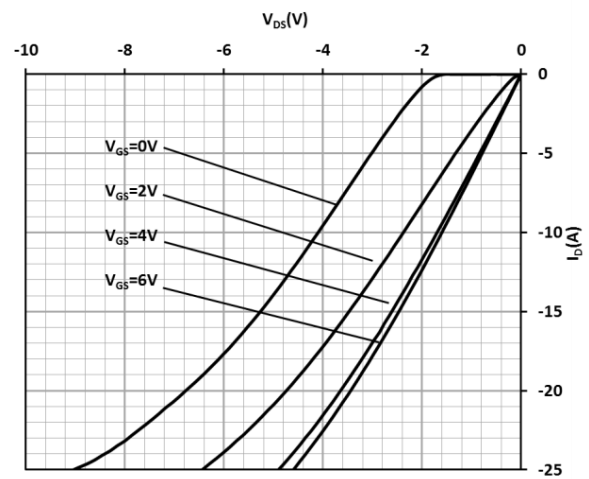
$$R_{DS(on)} = f(I_D, V_{GS}); T_j = 25\text{ }^\circ\text{C}$$

Figure 3 Typ. channel reverse characteristics



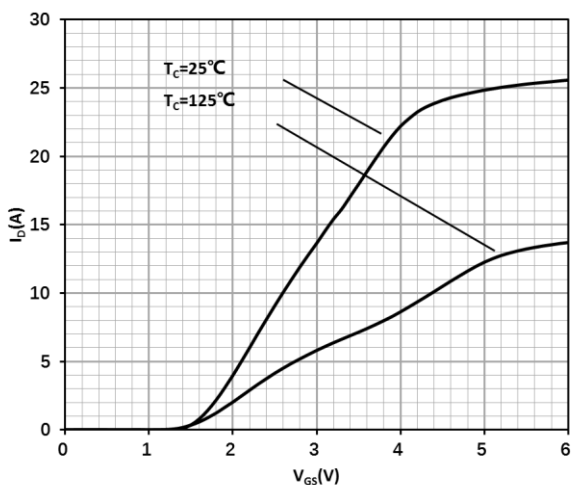
$$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^\circ\text{C}$$

Figure 4 Typ. channel reverse characteristics



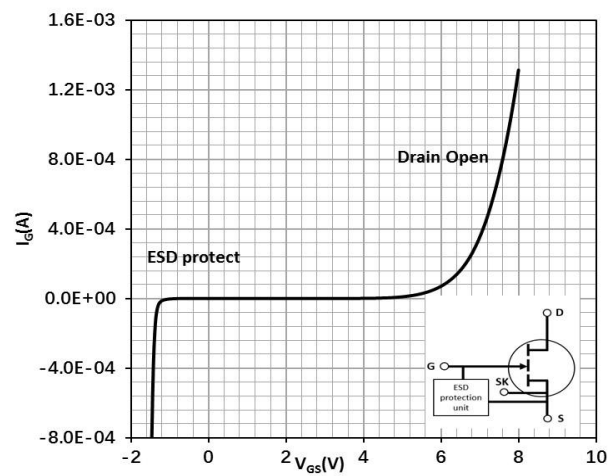
$$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^\circ\text{C}$$

Figure 5 Typ. transfer characteristics

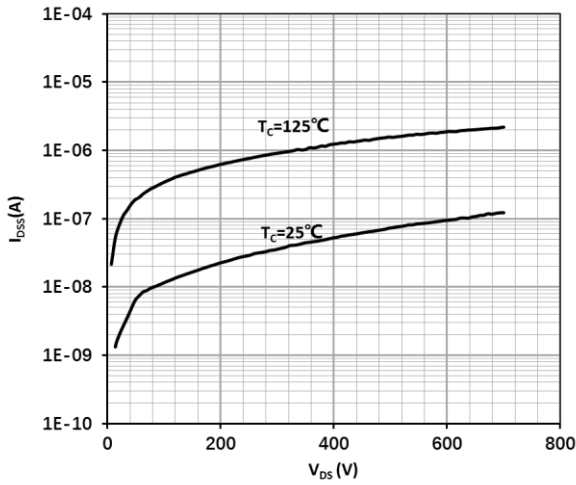


$$I_D = f(V_{GS}); V_{DS} = 3\text{ V}$$

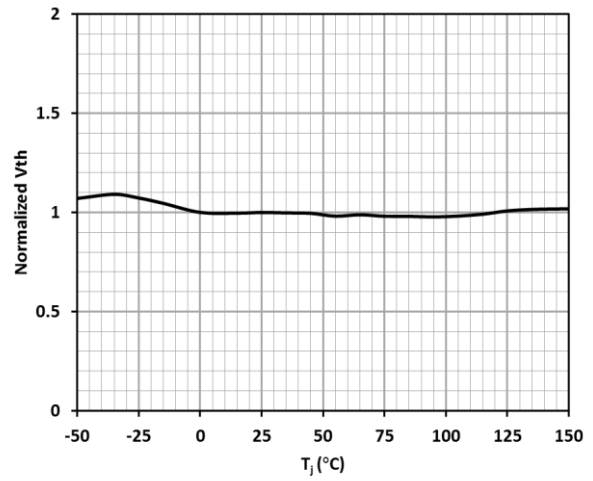
Figure 6 Typ. Gate-to-Source leakage



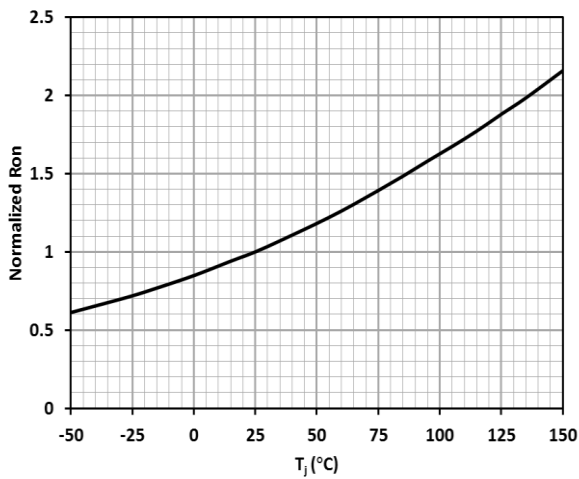
$$I_G = f(V_{GS}); I_G \text{ reverse turn on by ESD unit}$$

650V GaN Enhancement-mode Power Transistor
Figure 7 Drain-source leakage characteristics


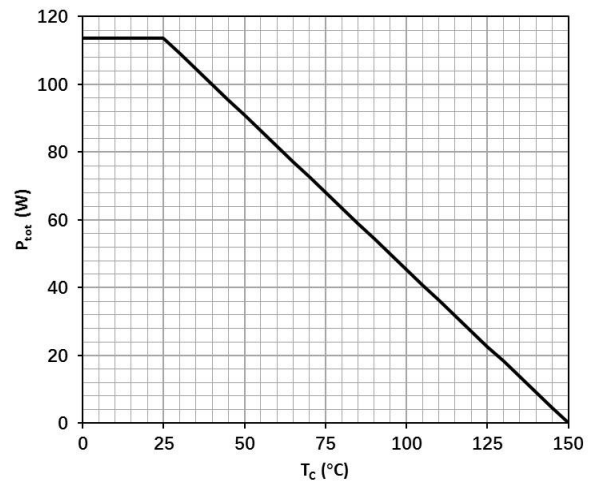
$$I_{DSS} = f(V_{DS}); V_{GS} = 0 \text{ V}$$

Figure 8 Gate threshold voltage


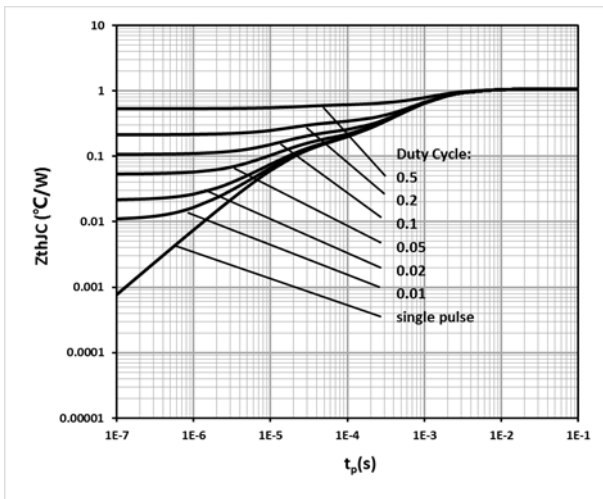
$$V_{TH} = f(T_j); V_{GS} = V_{DS}; I_D = 17.2 \text{ mA}$$

Figure 9 Drain-source on-state resistance


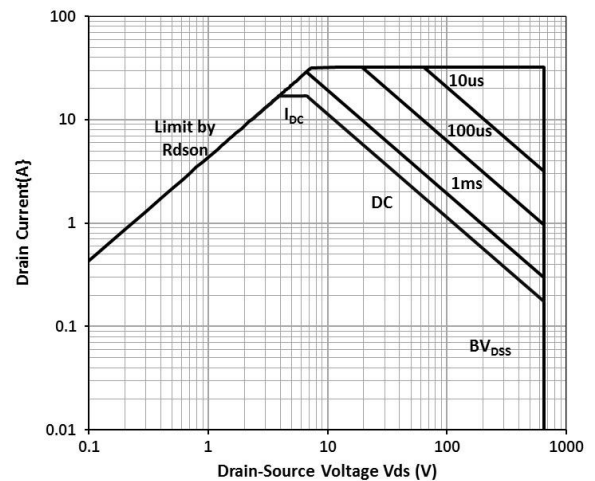
$$R_{DS(on)} = f(T_j); I_D = 5 \text{ A}; V_{GS} = 6 \text{ V}$$

Figure 10 Power dissipation


$$P_{tot} = f(T_c)$$

Figure 11 Max.transient thermal impedance


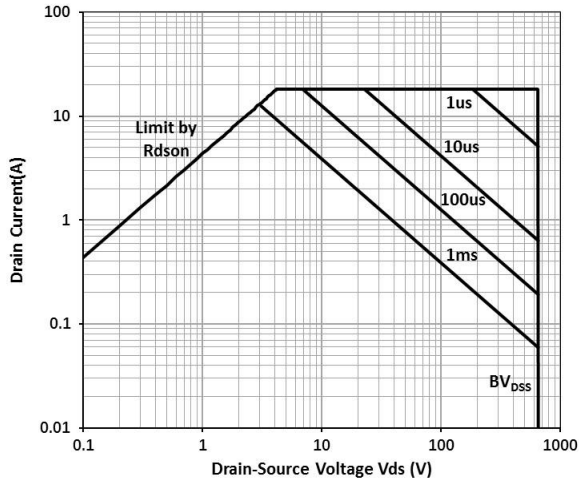
$$Z_{thJC} = f(t_p, D)$$

Figure 12 Safe operating area


$$I_D = f(V_{DS}); T_c = 25 \text{ °C}$$

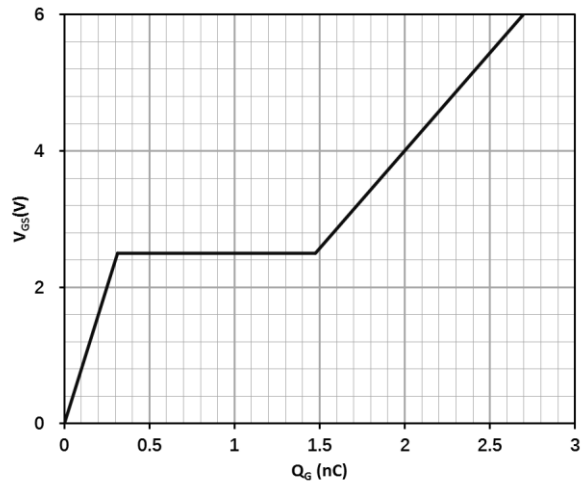
650V GaN Enhancement-mode Power Transistor

Figure 13 Safe operating area



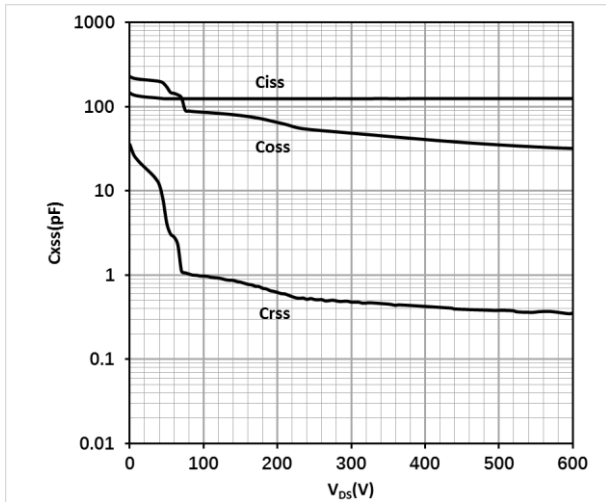
$$I_D = f(V_{DS}); T_c = 125^\circ\text{C}$$

Figure 14 Typ. gate charge



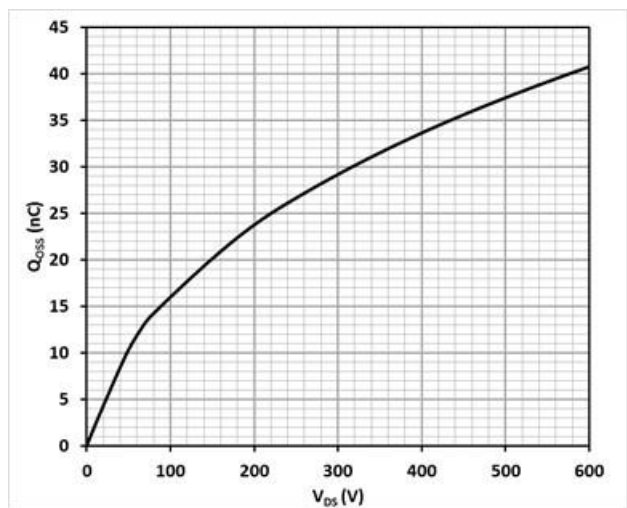
$$V_{GS} = f(Q_G); V_{DCLINK} = 400\text{ V}; I_D = 5\text{ A}$$

Figure 15 Typ. capacitances



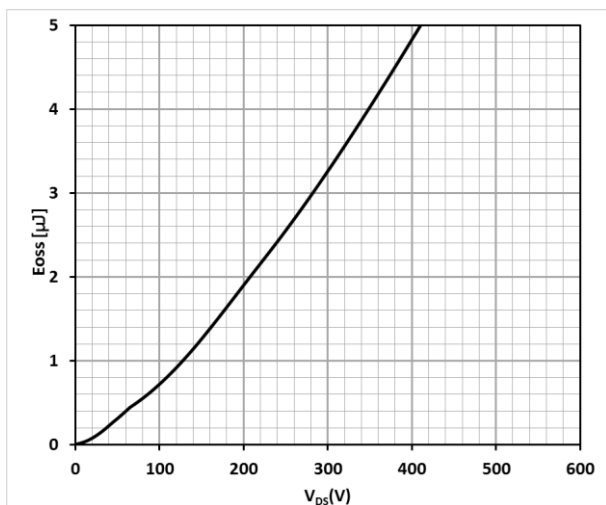
$$C_{XSS} = f(V_{DS}); \text{Freq.} = 100\text{ kHz}$$

Figure 16 Typ. output charge

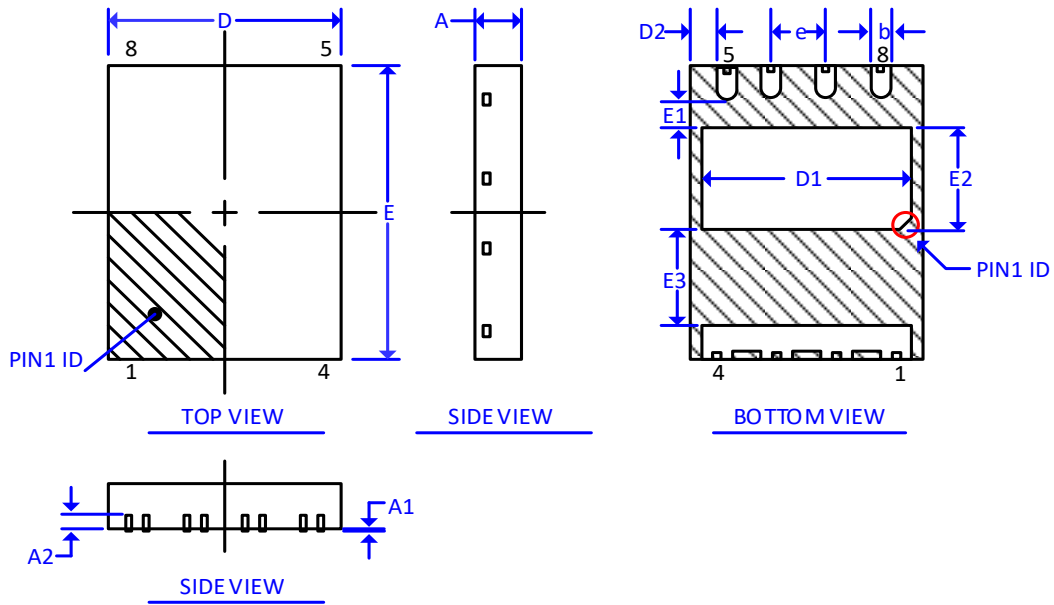


$$Q_{OSS} = f(V_{DS}); \text{Freq.} = 100\text{ kHz}$$

Figure 17 Typ. Coss stored Energy



$$E_{OSS} = f(V_{DS}); \text{Freq.} = 100\text{ kHz}$$

650V GaN Enhancement-mode Power Transistor
DFN5X6 Package Outline Dimensions


SYMBOL	DIMENSION			SYMBOL	DIMENSION		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.80	0.90	1.00	E	6.00 B.S.C		
A1	0.00	0.02	0.05	E1	0.40	0.50	0.60
A2	---	0.203 ref	---	E2	1.95	2.05	2.15
b	0.40	0.45	0.50	E3	---	2.1	---
D	5.00 B.S.C			e	1.27 B.S.C		
D1	4.16	4.26	4.36	L	0.575	0.675	0.775
D2	0.27	0.37	0.47				