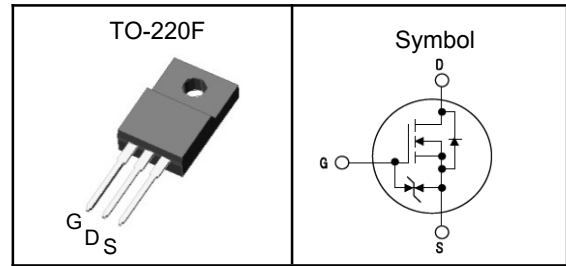


**650V Super Junction Power MOSFET**
**Features**

- Low drain-source on-resistance:  $R_{DS(ON)}=0.32\Omega(\text{typ})$
- Easy to control gate switching
- Enhancement mode:  $V_{th} = 2$  to  $4V$
- Built-in ESD Diode
- 100% avalanche tested

**Applications**

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- Charger, Lighting

**Pin Description**


$V_{DSS}$	650	V
$R_{DS(ON)-Typ}$	320	m $\Omega$
$I_D$	13	A

**Absolute Maximum Ratings** ( $T_J=25^\circ\text{C}$ , Unless Otherwise Noted)

Symbol	Parameter	Rating	Unit
$V_{DSS}$	Drain-Source Voltage	650	V
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$T_J$	Maximum Junction Temperature	-55 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Single Pulse Avalanche Energy <sup>③</sup>	320	mJ
$I_{DM}^{①}$	Pulse Drain Current Tested	33	A
$I_D$	Continuous Drain Current	$T_C=25^\circ\text{C}$	A
$P_D$	Maximum Power Dissipation	$T_C=25^\circ\text{C}$	W

**Thermal Characteristics**

Symbol	Parameter	Rating	Unit
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	62.5	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case	4	$^\circ\text{C}/\text{W}$

Note ① : Max. current is limited by bonding wire.

Note ② : UIS tested and pulse width are limited by maximum junction temperature  $150^\circ\text{C}$ .

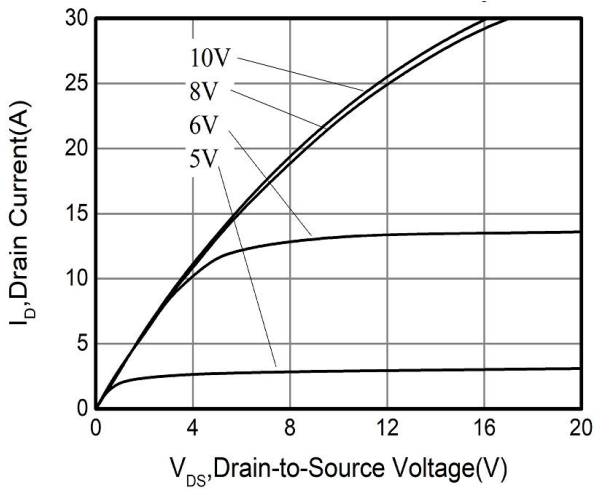
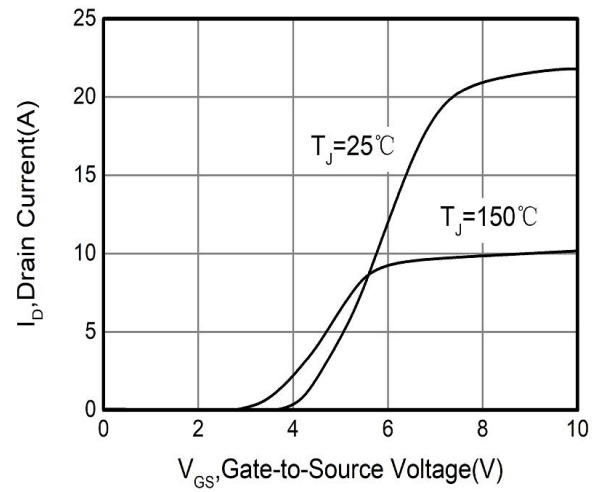
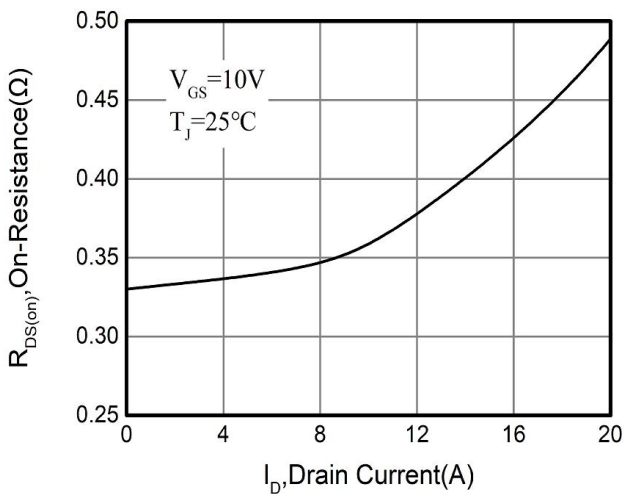
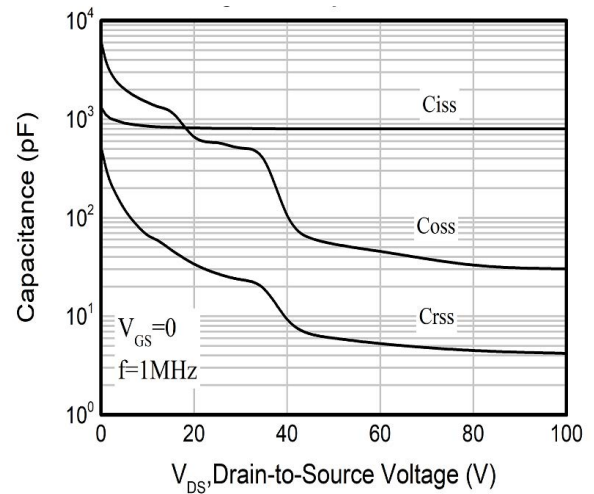
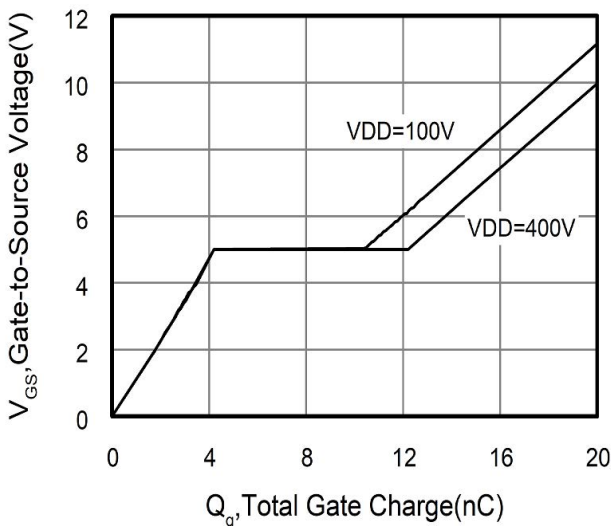
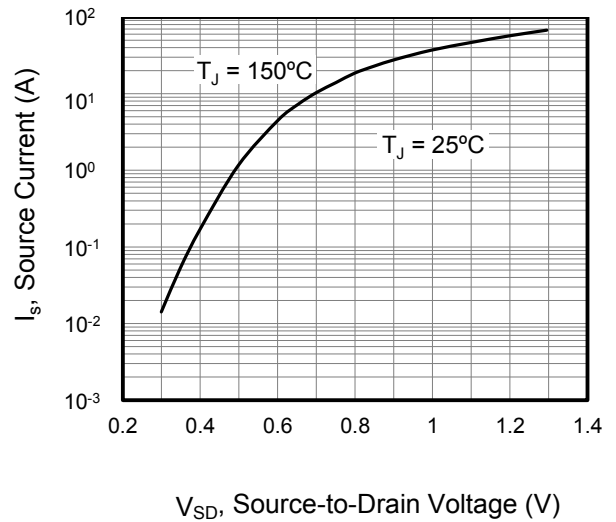
Note ③ : Surface Mounted on  $1\text{in}^2$  FR-4 board with 1oz.

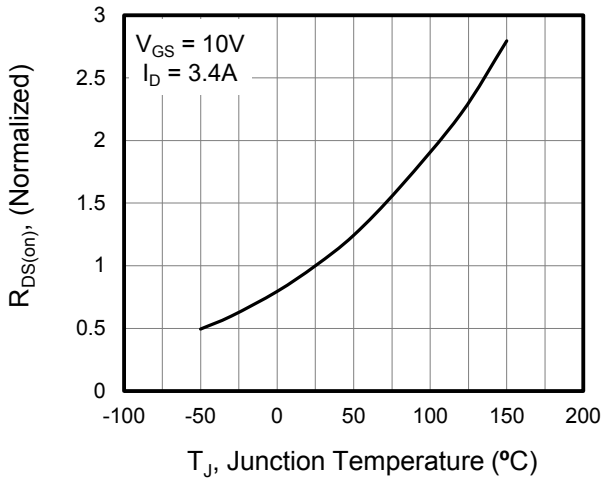
**650V Super Junction Power MOSFET****Electrical Characteristics** ( $T_J=25^\circ\text{C}$ , Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Static Electrical Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	---	---	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=600V, V_{GS}=0V$	---	---	1	$\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	---	4	V
$I_{GSS}$	Gate Leakage Current	$V_{GS}=\pm 30V, V_{DS}=0V$	---	---	$\pm 10$	$\mu A$
$R_{DS(ON)}$	Drain-Source On-state Resistance	$V_{GS}=10V, I_D=3.4A$	---	320	390	$m\Omega$
<b>Dynamic Characteristics</b> <sup>⑤</sup>						
$C_{iss}$	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=100V,$ Freq.=1MHz	---	860	---	pF
$C_{oss}$	Output Capacitance		---	30	---	
$C_{rss}$	Reverse Transfer Capacitance		---	4.2	---	
$T_{d(on)}$	Turn-on Delay Time	$V_{DD}=400V,$ $V_{GS}=10V, R_G=25\Omega,$ $I_D=4.8A$	---	41	---	nS
$T_r$	Turn-on Rise Time		---	20	---	
$T_{d(off)}$	Turn-off Delay Time		---	120	---	
$T_f$	Turn-off Fall Time		---	20	---	
$R_g$	Gate Resistance	$f = 1.0\text{MHz},$ open drain	---	13	---	$\Omega$
$Q_g$	Total Gate Charge	$V_{DS}=400V,$ $V_{GS}=10V, I_D=4.8A$	---	20	---	nC
$Q_{gs}$	Gate-Source Charge		---	4.2	---	
$Q_{gd}$	Gate-Drain Charge		---	7	---	
<b>Source-Drain Characteristics</b> ( $T_J=25^\circ\text{C}$ )						
$V_{SD}$ <sup>④</sup>	Diode Forward Voltage	$I_S=4.8A, V_{GS}=0V$	---	0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_R=400V, I_F=4.8A,$ $di/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	345	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	3.3	---	nC

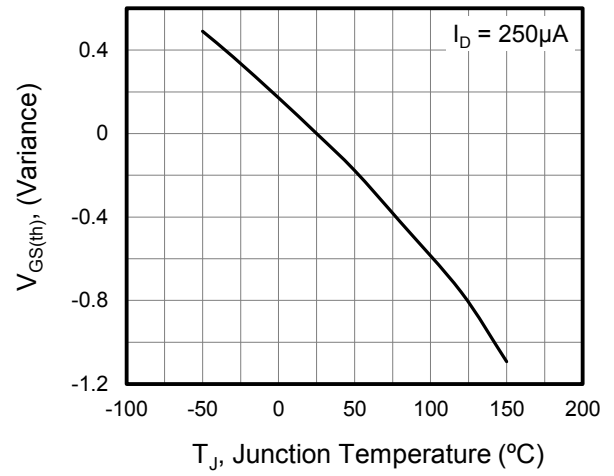
Note ④ : Pulse test (pulse width $\leq 300\mu s$ , duty cycle $\leq 2\%$ ).

Note ⑤ : Guaranteed by design, not subject to production testing.

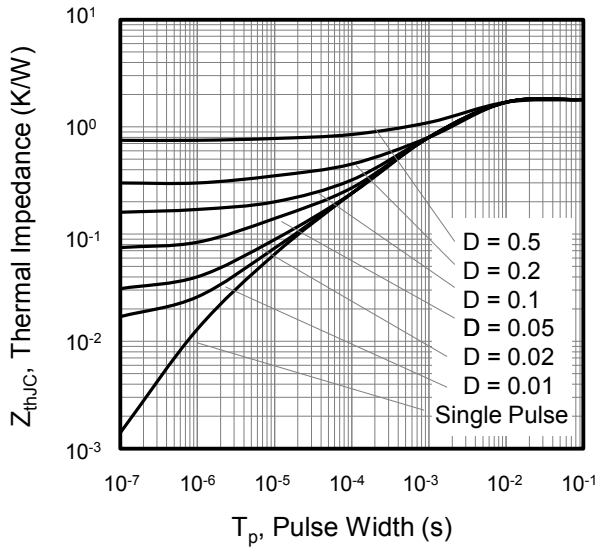
**650V Super Junction Power MOSFET**
**Typical Characteristics**

**Figure 1. Output Characteristics**

**Figure 2. Transfer Characteristics**

**Figure 3. On-Resistance vs. Drain Current**

**Figure 4. Capacitance**

**Figure 5. Gate-to-Source Voltage vs. Total Gate Charge**

**Figure 6. Body Diode Forward Voltage**

**650V Super Junction Power MOSFET**


**Figure 7. On-Resistance vs. Junction Temperature**



**Figure 8. Threshold Voltage vs. Junction Temperature**



**Figure 9. Transient Thermal Impedance**

**650V Super Junction Power MOSFET**
**TO-220F Package Outline Data**

unit: mm

